**Shanghai IC High Skilled Talent Training Base**

**Shanghai Silicon Intellectual Property Trading Center Co., Ltd**

**IC system design and simulation**

**Training and enrollment brochures**

1. Training object
2. Personnel engaged in integrated circuit design(including fresh master's graduates).
3. Personnel engaged in IC Verification.
4. Staff engaged in FPGA design and silicon testing.
5. Training objectives
6. Master the use of the current mainstream verification language SystemVerilog in verification.
7. Proficient in validation methodology UVM.
8. Be able to apply SV to build a hierarchical verification platform independently.
9. It can independently use UVM to build a complete module level verification platform.
10. Be able to conduct case operation in combination with verification methodology and SV, fully master design specifications, formulate verification scheme, complete verification platform construction, develop test cases, verification execution and coverage acceptance.
11. Refer to the verification process of first-class companies in the industry, and be able to complete relevant documents and pass the defense one by one.
12. Training features
13. Pay attention to the combination of theory and practice, focus on practical training skills, combine complete basic theoretical training, and guide practical training with reference to the verification process of front-line companies.
14. Formulation of verification scheme: including sorting and deconstruction of design specifications, selection of verification methods and platforms, including generation of incentives, design of reference models, random strategies, self comparison strategies, coverage assurance, verification complexity and guarantee of development progress, etc. The verifier needs to prepare relevant documents for defense to cultivate the ability to independently undertake the verification of complex modules.
15. Convergence of verification coverage: including full coverage of product specifications and test cases, as well as functional coverage and code coverage, so that students can pass verification and acceptance according to strict processes.
16. Training teachers

The training teachers and staff of the project are senior experts who have more than 10 years of expertise in IC Verification, and have experience in verification, project management and team leadership of complex SOC.

* Jimmy Peng: with 10 years of relevant experience in verification, the project scale is more than ten million dollar, and the process is 14 / 16nm / 20nm. The product involves the core chip of mobile phone, wireless communication and multimedia terminal. The IP involved includes: WCDMA, GSM, TD, WiFi, USB2, usb3, Mipi, CSI / DSI, CE, SD, SDIO, PCIe, EMMC, audio and video core algorithm IP; And low power consumption and power simulation at SOC level.
* Will Zhang: he has about ten years of verification experience, is proficient in various mainstream verification technologies and methodologies, leads the team in IP level and SOC level verification, and is responsible for the maintenance and development of verification process.
* Michael he: the project scale is more than ten million, and the process is 40 / 28nm. The products include base station baseband chip and Wi Fi mobile chip. The collectives involved include: multi-layer bus matix, multi-core ARM CPU, DDR3, etc., as well as low-power verification.

1. Syllabus

Theoretical teaching content

Training module 1: Fundamentals of SystemVerilog language

1.1 learning and mastering data types

1.1.1 embedded basic data type

1.1.2 fixed size array

1.1.3 dynamic arrays

1.1.4. Be able to correctly understand and master the queue

1.1.5 enumeration type

1.1.6 use of 6 characters

1.1.7 constant

1.1.8 create new types and data structures

1.2 process statements and programs

1.2.1 procedure statements introduction

1.2.2 understand and master the task

1.2.3 understand and master functions

1.2.4 definition and use of time

1.2.5 parameter transfer of program

1.2.6 Introduction to the interface of 6systemverilog

Training module 2: architecture of SystemVerilog TB

2.1.1 Introduction to the concept of hierarchical verification environment

2.1.2 TB package for DUT

2.1.3 construction of 3interface

2.1.4 driving and sampling of 4interface

2.1.5 definition of data structure

2.1.6 management of random number and data generation

2.1.7 preliminary introduction to the generation of incentive

2.1.8 timing management of incentive

2.1.9 basic functions of 9TB top layer

2.1.10 ATM router instance with four interfaces

Training module 3: UVM validation methodology

3.1.1 Introduction to UVM verification methodology

3.1.2 Key points of each part of UVM verification environment

3.1.3 uvm driver key points

3.1.4 uvm sequencer key points

3.1.5 uvm monitor Essentials

3.1.6 uvm Vif key points

3.1.7 uvm phase key points

3.1.8 uvm TLM interface points

3.1.9 uvm ral key points

3.1.10 Integration of 10uvm environment

3.1.11 Application example analysis of typical UVM verification environment of 11 router

Training module 4: UVM verification environment training

4.1.1 verify the architecture of the environment

4.1.2 Definition and implementation of 2uvm transaction

4.1.3 tlm communication, put, get, analysis port

4.1.4 be able to master the implementation method of UVM driver

4.1.5. Be able to master the implementation method of UVM sequencer

4.1.6. Be able to master the implementation method of UVM monitor

4.1.7. Be able to master the implementation method of UVM agents

4.1.8 design points of general router

4.1.9 general I2C design points

content of skill training

Training module 1: Fundamentals of SystemVerilog language

1. Definition, assignment and cyclic printing of SV basic data type

2. Array declaration, assignment and printing, including single-dimensional and multi-dimensional arrays

3. Implement the task of a simple adder and write a simple TB to debug the task

4. Function implementation, and debugging

5. Debug the task and pass the parameters of the function

6. Build a simple TB for the router and use the interface to package the DUT

Training module 2: architecture of SystemVerilog TB

1. Debugging of ATM router instance with four interfaces

2. Develop TB to package DUT

3. Define data interface

4. Implement interfaces and generate incentives

5. Manage TB timing

Training module 3: UVM validation methodology

1. Develop a complete UVM verification environment for router

2. Practically develop all UVM components driver, monitor and sequencer

3. Define TLM interface, Vif

4. Complete environment integration

5. Debug

Training module 4: UVM verification environment training

1. Develop a complete UVM verification environment for router

2. Practically develop all UVM components driver, monitor and sequencer

3. Define TLM interface, Vif

4. Complete environment integration

5. Debug

1. Training plan

1、Total training hours: 26 theoretical courses and 54 practical courses, totaling 80 hours

2、Online course opening form: course platform, course viewing cycle is 3 months, including the use time of training account for 1 month.

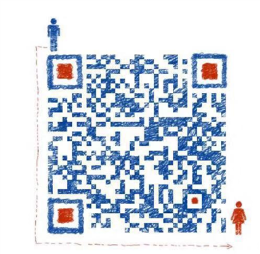
3、Opening time: online courses are open at any time, unlimited number of people; offline courses enrollment begins when classes were full.

1. Contact information

Contacts：Gina Hong/021-61154610 Cherie Su/021-61154610

E-mail：gina.hong@ssipex.com cherie.su@ssipex.com

Wechat：

\*Please refer to the Chinese version for the contents of enrollment brochures!

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