**Shanghai IC High Skilled Talent Training Base**

**Shanghai Silicon Intellectual Property Trading Center Co., Ltd**

**IC Integrated circuit Layout Design**

**Training and enrollment brochures**

1. Training object
2. Science and engineering graduates with zero foundation of integrated circuit layout design (including microelectronics, physics, materials, computer and other related majors).
3. Relevant professionals who are willing to engage in integrated circuit layout design.
4. Training objectives

Junior Engineer: through the training, the zero foundation students fully master the knowledge and skills of IC layout design, become a qualified junior engineer and can undertake ordinary IC layout design.

1. Training features
2. Shanghai Silicon Intellectual Property Trading Center has a national excellent territory learning platform and hardware support, including the most advanced design tools and verification tools.
3. In order to ensure the training quality, learning courses and practical training are mainly offline, and homework, Q & A and extracurricular learning are assisted online.
4. Training teachers
* William Kin: he has nearly 17 years of experience in integrated circuit layout design, has full process layout design technology, and has long-term experience as a project director in top enterprises such as Qualcomm. At present, he is a senior manager of the layout group of an emerging chip design company, has established a 20 person layout team, led the layout of nearly 10 super large-scale chips, and all of them have been successfully mass produced.
1. Syllabus
2. Basic course of integrated circuit layout design
3. Concept and development prospect of integrated circuit
4. Integrated circuit manufacturing process flow
5. Integrated circuit and integrated circuit layout design
6. IC layout design process
7. Layout design environment
8. Linux operating system
9. Linux instruction compact
10. VI instruction operation
11. 4. Know PDK
12. Process document, rule interpretation
13. Working environment settings
14. Detailed explanation of layout tools
15. Layout design tool
16. Dispay and bindkey files
17. Detailed explanation of verification tools
18. Figure operation shortcut keys
19. Devices and units in integrated circuit design
20. Active and passive components: MOS tube, diode, bipolar, resistance, capacitance, inductance, etc
21. Interconnection contact, via
22. Basic concept and layout implementation of MOS transistor and standard digital logic
23. Basic concept and graphic understanding of CMOS
24. Detailed explanation of CMOS layout
25. Common skills of CMOS layout
26. Layout design and verification of standard digital units (inv / nand2 / nor2 / nand3 / nor3 / OSC)
27. Layout design specification
28. Layout match concept and device matching
29. ESD layout design
30. Latch up effect
31. Parasitic effect
32. Antenna effect
33. Guard ring
34. Isolation shielding
35. Reliability rule
36. Metal density rule
37. Electromigration effect
38. Packaging
39. Netlist knowledge netlist
40. Simulated layout design employment practice
41. Layout design and practice of differential amplifier
42. Comp layout design practice
43. VCO layout design
44. RF layout design
45. Layout design of power transistor
46. Layout design of PLL
47. Bandgap layout design
48. SerDes high speed layout design
49. Top layout
50. Fullchip
51. floorplan
52. Chip design process
53. Training plan

1. Total online training hours: 24 Theoretical Courses and 56 practical training courses, totaling 80 hours

2. Online course opening form: course platform, course viewing cycle is 3 months, including training account, use time is 1 month, and development board is not provided;

Offline courses: 8 class hours per day for 10 weeks on weekends;

3. Opening time: online courses are open at any time, unlimited number of people; Offline courses began to recruit students, and classes were full

1. Contact information

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Wechat：

  

\*Please refer to the Chinese version for the contents of enrollment brochures!

January -2022