**Shanghai IC High Skilled Talent Training Base**

**Shanghai Silicon Intellectual Property Trading Center Co., Ltd**

**Digital circuit layout and wiring design (PR)**

**Training and enrollment brochures**

1. Training object
2. Junior designers engaged in IC back-end design and Implementation (including fresh master graduates(including fresh master's graduates).
3. Microelectronics industry practitioners interested in digital circuit layout and wiring design.
4. Training objectives
5. Master the current mainstream back-end layout and wiring tool.
6. Master the back-end layout and wiring method.
7. Be able to use circuit design and simulation tools.
8. It can independently complete the implementation process of back-end layout and wiring from net-list to GDSII.
9. Training features
10. Pay attention to the combination of theory and practice, focus on practical training skills, combine complete basic theoretical training, and guide practical training with reference to the verification process of front-line companies.
11. Formulation of physical implementation scheme: including data preparation, layout planning, clock tree synthesis and cabling design. Train designers to master the actual design process and cultivate the ability to independently undertake complex layout and wiring design.
12. Timing verification and physical verification: including static timing analysis process and physical verification DRC / LVS / ant / DFM process and inspection methods, so that students can master the strict verification process.
13. Training teacher

* Mr. Chen, a senior R & D Engineer in a well-known foreign enterprise, has an in-depth understanding of icc2 optimization algorithm and implementation framework, has experience in C + + algorithm development, has rich experience in 14 / 28 mm physical layout design and streaming, is good at analyzing and solving various types of timing winding problems encountered in the project, and has rich experience in script language development and automation process design.

1. Syllabus

Training unit 1: digital circuit layout and wiring data planning preparation

1. Main contents of training

(1) Theoretical teaching content

1.1.1 definition of physical library

1.1.2 definition of timing library

1.1.3 definition of net-list Library

1.1.4 EDA user manual

1.1.5 I / O placement requirements and constraint methods

1.1.6 chip layout (placement of ram, ROM, etc.)

1.1.7 definition of power loop and power strip

(2) Skill training content

1.2.1 prepare library files for standard units, macro units and I / O pads

1.2.2 check the timing constraint file and confirm the necessary clock definitions in the constraint file.

1.2.3. Check the correctness of door level net list

1.2.4 properly start EDA tools

1.2.5 place the I / O interface unit and I / O power supply unit

1.2.6. Complete layout planning scheme and delay estimation

1.2.7 design power network with EDA tools

Training unit 2 : digital circuit layout, wiring, clock tree synthesis and automatic layout design

1. Main contents of training

(1) Theoretical teaching content

2.1.1 definition of clock signal

2.1.2 definition of clock signal delay jitters and deviation

2.1.3 clock tree structure

2.1.4 clock tree constraint file and design method

2.1.5 clock tree and time series analysis method

2.1.6 clock tree and power analysis method

2.1.7 clock tree and noise analysis method

2.1.8 layout method of standard unit

2.1.9 clock tree and reset tree synthesis method

2.1.10 virtual wiring method

2.1.11 Methods to optimize timing, reduce coupling effect, eliminate crosstalk, reduce power consumption and ensure signal integrity

2.1.12 scan chain definition and reorganization method

(2) Skill training content

2.2.1 use EDA tool to set relevant parameters of clock tree synthesis and complete clock tree synthesis

2.2.2 use EDA tools to do the design strategy of clock tree

2.2.3 use EDA tool to analyze the comprehensive results of clock tree

2.2.4 use EDA tools to complete the circuit unit layout design according to the timing geometry model of the basic unit library

2.2.5 use EDA tool to complete the reorganization of scanning chain

Training unit 3: automatic wiring design of digital circuit

1. Main contents of training

(1) Theoretical teaching content

3.1.1 global cabling objectives and planning

3.1.2 detailed cabling objectives and planning

3.1.3 wiring correction method

3.1.4 clock tree wiring method

3.1.5 bus wiring method

1. Skill training content

3.2.1 use ICC tools to set global wiring parameters and complete global wiring

3.2.2 use ICC tools to set detailed wiring parameters and complete detailed wiring

3.2.3 use ICC tools to set other special wiring parameters and complete other special wiring (such as bus wiring and shielded interference wiring)

Training unit 4: verification and physical verification of timing performance of digital circuit

1. Main contents of training

(1) Theoretical teaching content

4.1.1 parasitic parameter concept

4.1.2 circuit design tool user manual

4.1.3 timing analysis and optimization method

4.1.4 circuit simulation tool user manual

4.1.5 method for checking the difference between the integrated net list and the net list after layout and wiring

4.1.6 validation tool A user manual

4.1.7 validation tool B user manual

4.1.8 method of checking DRC by design rules

4.1.9 implementation method of improving yield

4.1.10 LVS is a method to ensure the consistency between the function of layout file and the original circuit design function

(2) content of skill training

4.2.1 use EDA tool to set the parasitic parameter information of extraction wiring and generate SPEF files containing parasitic parameters

4.2.2 use EDA tools to set parameters required for static timing analysis, complete timing analysis and master optimization methods.

4.2.3 use EDA tools to set the parameters required for formal verification, complete the formal verification of functions, and ensure the correctness of net-list functions.

4.2.4 use EDA tools, set corresponding tool parameters according to process requirements, and complete physical verification (DRC / LVS / DFM)

1. Training plan

1. Total online training hours: 24 Theoretical Courses and 56 practical training courses, totaling 80 hours

2. Online course opening form: course platform, course viewing cycle is 3 months, including training account, use time is 1 month, and development board is not provided;

Offline courses: 8 class hours per day for 10 weeks on weekends;

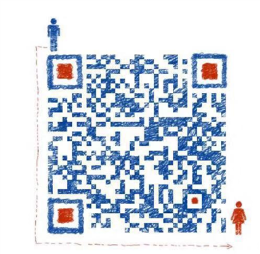
3. Opening time: online courses are open at any time, unlimited number of people; Offline courses began to recruit students, and classes were full

1. Contact information

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\*Please refer to the Chinese version for the contents of enrollment brochures!

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