**Shanghai IC High Skilled Talent Training Base**

**Shanghai Silicon Intellectual Property Trading Center Co., Ltd**

**Mirco-chip testability circuit design and simulation (DFT)**

**Training and enrollment brochures**

1. Training object
2. Personnel engaged in integrated circuit design(including fresh master's graduates).
3. Staff interested in integrated circuit DFT design and verification.
4. Training objectives
5. Understand the basic concept of IC testing, the basic principle of design for testability, and be familiar with the mainstream design for testability methods in the industry.
6. Master the boundary scan technology and be able to independently design the required hardware logic.
7. Master scan insertion technology and understand common fault tests such as stuck at, transit, path delay and IDDQ.
8. Understand the significance of on-chip clock control (OCC) for at speed test, and understand and master scan compression technology.
9. Master ATPG implementation technology, generate and verify test vectors.
10. Master MBIST implementation technology, perform MBIST logic insertion and verification.
11. Be able to combine the learned test methodology, design the testability structure of SOC chip, formulate test scheme, realize test structure, verify test results, collect coverage and estimate yield.
12. Understand the significance of MBIST diagnosis and scan diagnosis for improving chip manufacturing yield, and master the basic test and diagnosis process.
13. Be able to refer to the testable design verification process of first-class companies in the industry, complete relevant documents and pass the defense one by one.
14. Training features

1. It is characterized by paying attention to the combination of theory and practice, focusing on practical training skills, combined with complete basic theoretical training, and guiding practical training with reference to the testable design verification process of front-line companies.

2. Testable methodology: it covers the implementation of testable methods for different modules in complex SOC, including boundary scan test for pad test, scan chain test for digital logic, and self-test method for memory.

3. Formulation of testable scheme: including the formulation of test objectives and requirements, the selection of test methods and platforms, the generation and verification of test incentives, coverage assurance, yield analysis, test cost estimation and development progress assurance, etc. Testable developers need to prepare relevant documents for defense to cultivate the ability to independently undertake complex chip testing.

4. Convergence of testable coverage: it includes the collection of testable coverage, methods to improve testable coverage, and the impact of testable coverage on the yield of final products, so that students can pass the acceptance of testable results according to strict procedures.

1. Training teachers

Jacky Yang, a senior expert specializing in IC Verification for more than 10 years, has experience in testable design verification, project management and team leadership of complex SOC.Syllabus

Training unit 1: chip testability circuit design simulation work method planning and formulation

1. Syllabus

Training unit 1: Planning and formulation of working methods for chip testability circuit design and simulation

(1) Theoretical teaching content

1.1 basic concept of test circuit

1.2 chip test process

1.3 automatic test equipment

1.4 testable design concept

1.5 testable design method

1.6 fault modeling

1.7 common fault model

（2）Skill training content

2.1 find the failure point by using the fault inspection algorithm

2.2 select the testable method corresponding to the circuit design according to the different functions of the chip

Training unit 2: boundary scan testability circuit design and verification

(1) Theoretical teaching content

1.1 principle of JTAG

1.2 boundary scan register structure

1.3 boundary scan register instruction

1.4 boundary scan language definition

1.5 verification method of JTAG circuit

(2) Skill training content

2.1 JTAG circuit design using Verilog, TCL, shell and Perl design languages

2.2 understand boundary scan language and design boundary scan circuit according to boundary scan language

2.3 verify JTAG and boundary scan circuit with timing simulation tool

Training unit 3: Design and verification of scan chain testability circuit

(1) Theoretical teaching content

1.1 basic principle of scan chain circuit

1.2 principle of ATPG (automatic excitation generation)

1.3 basic process of scan chain circuit design

1.4 EDA tools related to scan test

1.5 scan chain insertion related logic functions

1.6 basic process of scan chain insertion

1.7 basic commands and functions of scan chain insertion

1.8 basic process of ATPG (automatic excitation generation)

1.9 ATPG test vector type

1.10 basic commands and functions realized by ATPG

1.11 ATPG design rule inspection

1.12 ATPG fault type

1.13 coverage calculation

1.14 scan chain circuit verification

1.15 scan chain circuit commissioning

(2) Skill training content

2.1 using test tools to realize scan chain circuit and integration

2.2 using test tools to generate automated test vectors

2.3 DRC specification inspection with test tools

2.4 calculate the coverage by using test tools

2.5 verify the scan chain circuit by using the timing simulation tool

Training unit 4: Design and verification of memory cell built-in testability circuit test method

Main contents of training

(1) Theoretical teaching content

1.1 memory structure

1.2 ram failure

1.3 built in self-test method

1.4 common built-in self-test algorithms

1.5 principle of built-in self-test circuit

1.6 design rule inspection of built-in self-test

1.7 design planning of built-in self-test

1.8 design and implementation of built-in self-test

1.9 verification of built-in self-test

(2) Skill training content

2.1 use tool design language to design the built-in self-test circuit of storage unit

2.2 verify the built-in self-test circuit of storage unit by using timing simulation tool

1. Training plan

1. Total online training hours: 24 Theoretical Courses and 56 practical training courses, a total of 80 hours;

2. Online course opening form: course platform, course viewing cycle is 3 months, including the use time of training account for 1 month;

Offline courses: 8 class hours per day for 10 weeks on weekends;

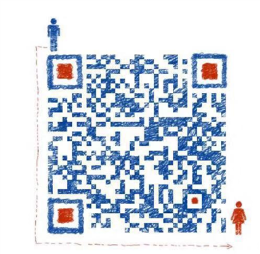
3. Opening time: online courses are open at any time, unlimited number of people; Offline courses are full;

1. Contact information

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\*Please refer to the Chinese version for the contents of enrollment brochures!

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